MIC5022

Half-Bridge MOSFET Driver

General Description

The MIC5022 half-bridge MOSFET driver is designed to operate at frequencies up to 100kHz (5kHz PWM for 2% to 100% duty cycle) and is an ideal choice for high speed applications such as motor control and SMPS (switch mode power supplies).

A rising or falling edge on the input results in a current source pulse or sink pulse on the gate outputs. This output current pulse can turn on a 2000pF MOSFET in approximately 1µs. The MIC5022 then supplies a limited current (< 2mA), if necessary, to maintain the output states.

Two overcurrent comparators with nominal trip voltages of 50mV make the MIC5022 ideal for use with current sensing MOSFETs. External low value resistors may be used instead of sensing MOSFETs for more precise overcurrent control. Optional external capacitors placed on the C_{TH} and C_{TL} pins may be used to individually control the current shutdown duty cycles from approximately 20% to <1%. Duty cycles from 20% to about 75% are possible with individual pull-up resistors from C_{TL} and C_{TH} to V_{DD}. An open collector output provides a fault indication when either sense input is tripped.

The MIC5022 is available in 16-pin wide SOIC and 14-pin plastic DIP packages.

Other members of the MIC502x family include the MIC5020 low-side driver and the MIC5021 high-side driver.

Features

- 12V to 36V operation
- 600ns rise time into 1000pF (high side)
- TTL compatible input with internal pull-down resistor
- Outputs interlocked to prevent cross conduction
- TTL compatible enable
- Fault output indication
- Individual overcurrent limits
- Gate protection
- Internal charge pump (high-side)
- Current source drive scheme reduces EMI

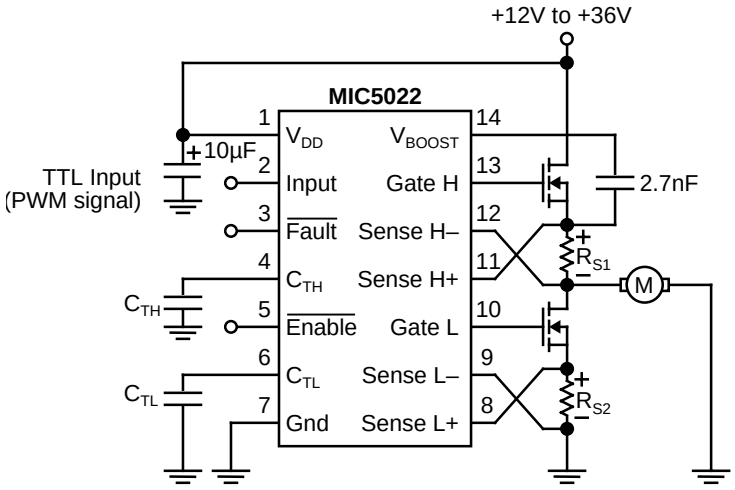
Applications

- Motor control
- Switch-mode power supplies

Ordering Information

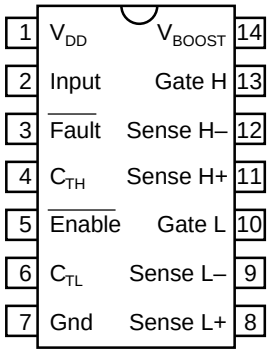
Part Number	Temperature Range	Package
MIC5022BWM	–40°C to +85°C	16-pin Wide SOIC
MIC5022BN	–40°C to +85°C	14-pin Plastic DIP

Typical Application

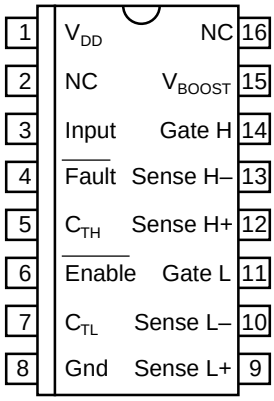


DC Motor Control Application

Pin Configuration



DIP Package (N)

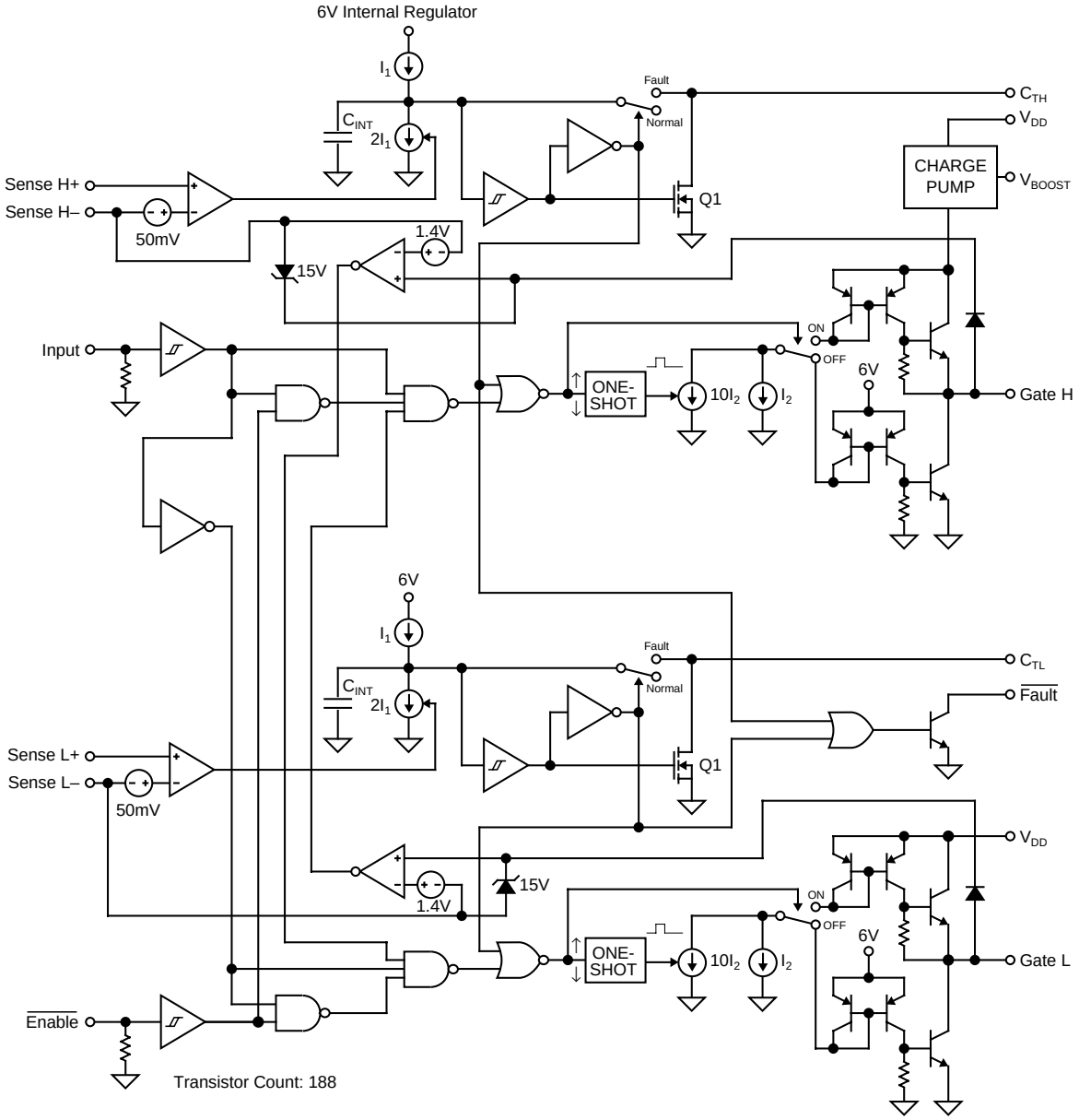


SOIC Package (WM)

Pin Description

DIP Pin No.	SOIC Pin No.	Pin Name	Pin Function
1	1	V_{DD}	Supply: +12V to +36V. Decouple with ≥ 10µF capacitor.
2	3	Input	TTL Compatible Input: Logic high turns the high-side external MOSFET on and the low-side external MOSFET off. Logic low turns the high-side external MOSFET off and the low-side external MOSFET on. An internal pull-down returns an open pin to logic low.
3	4	$\overline{Fault}$	When either sense voltage exceeds threshold, open collector output is open circuit for 5µs ($t_{G(ON)}$), then pulled low for $t_{G(OFF)}$. $t_{G(OFF)}$ is adjustable from C_T.
4	5	C_{TH}	Retry Trimming Capacitor, High Side: Controls the off time ($t_{G(OFF)}$) of the overcurrent retry cycle. (Duty cycle adjustment.) • Open = approx. 20% duty cycle. • Capacitor to Ground = approx. 20% to < 1% duty cycle. • Pullup resistor = approx. 20% to approx. 75% duty cycle. • Ground = maintained shutdown upon overcurrent condition.
5	6	$\overline{Enable}$	Output Enable: Disables operation of the output drivers; active high. An internal pull-down returns an open pin to logic low.
6	7	C_{TL}	Retry Trimming Capacitor, Low Side: Same function as C_{TH}.
7	8	Gnd	Circuit Ground
8	8	Sense L +	Current Sense Comparator (+) Input, Low Side: Connect to source of low-side MOSFET. A built-in offset (nominal 50mV) in conjunction with R_{SENSE} sets the load overcurrent trip point.
9	10	Sense L –	Current Sense Comparator (–) Input, Low Side: Connect to the negative side of the low-side sense resistor.
10	11	Gate L	Gate Drive, Low Side: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.
11	12	Sense H +	Current Sense Comparator (+) Input, High Side: Connect to source of high-side MOSFET. A built-in offset (nominal 50mV) in conjunction with R_{SENSE} sets the load overcurrent trip point.
12	13	Source H –	Current Sense Comparator (–) Input, High Side: Connect to the negative side of the high-side sense resistor.
13	14	Gate H	Gate Drive, High Side: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.
14	15	V_{BOOST}	Charge Pump Boost Capacitor: A bootstrap capacitor from V_{BOOST} to the MOSFET source pin supplies charge to quickly enhance the external MOSFET's gate .

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... +40V
Input Voltage ..... –0.5V to 15V
Sense Differential Voltage ..... ±6.5V
Sense + or Sense – to Gnd ..... –0.5V to +36V
$\overline{\text{Fault}}$ Voltage ..... +36V
Current into $\overline{\text{Fault}}$ 50mA
Timer Voltage (C_T) ..... +5.5V
V_{BOOST} Capacitor 0.01µF

Operating Ratings

Supply Voltage (V_{DD}) ..... +12V to +36V
Temperature Range
SOIC ..... –40°C to +85°C
PDIP ..... –40°C to +85°C

Electrical Characteristics

T_A = 25°C, Gnd = 0V, V_{DD} = 12V, Gate C_L = 1500pF (IRF540 MOSFET) unless otherwise specificed

Symbol	Parameter	Condition	Min	Typ	Max	Units
	D.C. Supply Current	V_{DD} = 12V, Input = 0V		2.5	5	mA
		V_{DD} = 36V, Input = 0V		6.0	10	mA
		V_{DD} = 12V, Input = 5V		2.4	5	mA
		V_{DD} = 36V, Input = 5V		3.0	25	mA
	Input Threshold		0.8	1.4	2.0	V
	Input Hysteresis			0.1		V
	Input Pull-Down Current	Input = 5V	10	20	40	µA
	$\overline{\text{Enable}}$ Threshold		0.8	1.4	2.0	V
	$\overline{\text{Enable}}$ Hysteresis			0.1		V
	Fault Output Saturation Voltage	Fault Current = 1.6mA **Note 1**		0.15	0.4	V
	Fault Output Leakage	Fault = 36V	–1	0.01	+1	µA
	Current Limit Thresh., Low-Side	**Note 2**	30	50	70	mV
	Current Limit Thresh., High-Side	**Note 2**	30	50	70	mV
	Gate On Voltage, High-Side	V_{DD} = 12V, **Note 3**	16	18	21	V
		V_{DD} = 36V, **Note 3**	46	49	52	V
	Gate On Voltage, Low-Side	V_{DD} = 12V, **Note 3**	10	11		V
		V_{DD} = 36V, **Note 3**	14	15	18	V
$t_{G(ON)}$	Gate On Time, Fixed	Sense Differential > 70mV	2	5	10	µs
$t_{G(OFF)}$	Gate Off Time, Adjustable	Sense Differential > 70mV, C_T = 0pF	10	20	50	µs
t_{DLH}	Gate Turn-On Delay, High-Side	**Note 4**		1.4	2.0	µs
t_R	Gate Rise Time, High-Side	**Note 5**		0.8	1.5	µs
t_{DHL}	Gate Turn-Off Delay, High-Side	**Note 6**		1.2	2.0	µs
t_F	Gate Fall Time, High-Side	**Note 7**		0.6	1.5	µs
t_{DLH}	Gate Turn-On Delay, Low-Side	**Note 4**		1.7	2.5	µs
t_R	Gate Rise Time, Low-Side	**Note 8**		0.7	1.5	µs
t_{DHL}	Gate Turn-Off Delay, Low-Side	**Note 9**		0.5	1.0	µs
t_F	Gate Fall Time, Low-Side	**Note 10**		1.0	1.5	µs

Note 1 Voltage remains low for time affected by C_T.

Note 2 When using sense MOSFETs, it is recommended that R_{SENSE} < 50Ω. Higher values may affect the sense MOSFET's current transfer ratio.

Note 3 DC measurement.

Note 4 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 0V to 2V.

Note 5 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 17V.

Note 6 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 20V (Gate on voltage) to 17V.

Note 7 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 17V to 2V.

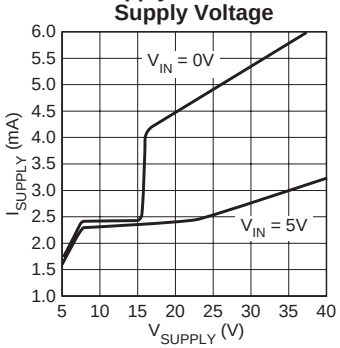
Note 8 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 10V.

Note 9 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 15V (Gate on voltage) to 10V.

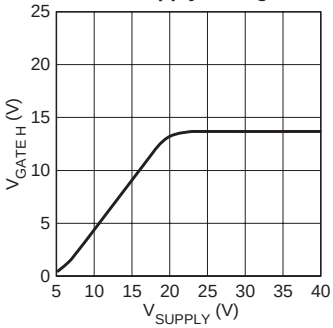
Note 10 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 10V to 2V.

Typical Characteristics

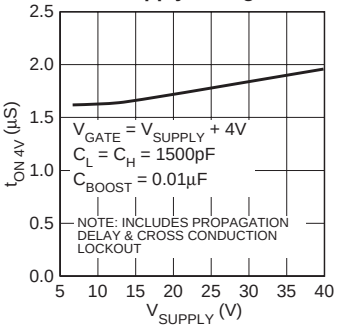
Supply Current vs. Supply Voltage



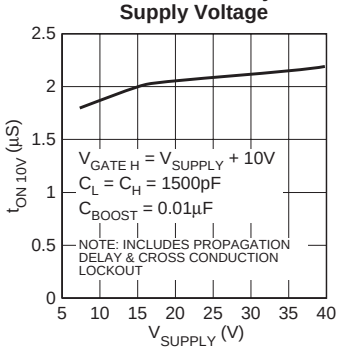
Gate to Source Voltage vs. Supply Voltage



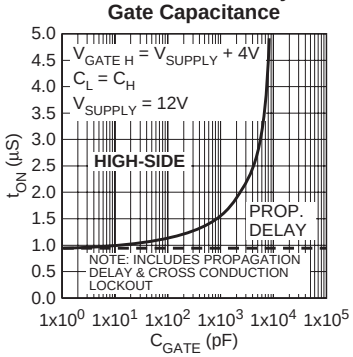
Gate Turn-On Delay vs. Supply Voltage



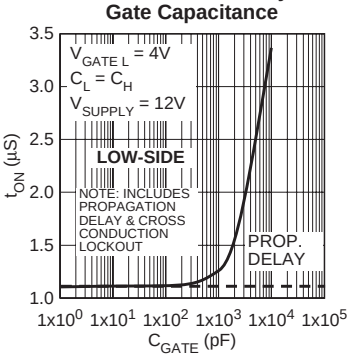
Gate Turn-On Delay vs. Supply Voltage



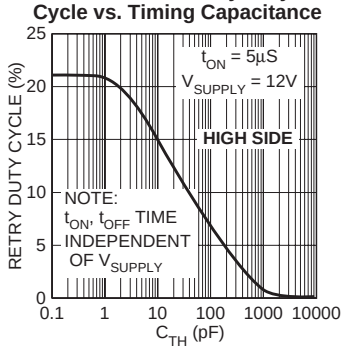
Gate Turn-On/Off Delay vs. Gate Capacitance



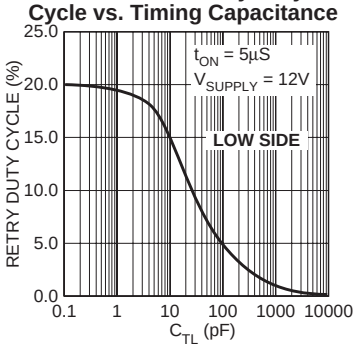
Gate Turn-On/Off Delay vs. Gate Capacitance



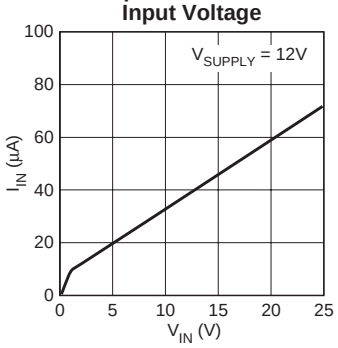
Overcurrent Retry Duty Cycle vs. Timing Capacitance



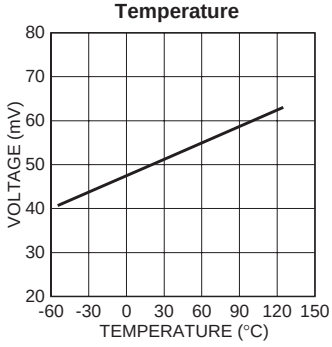
Overcurrent Retry Duty Cycle vs. Timing Capacitance

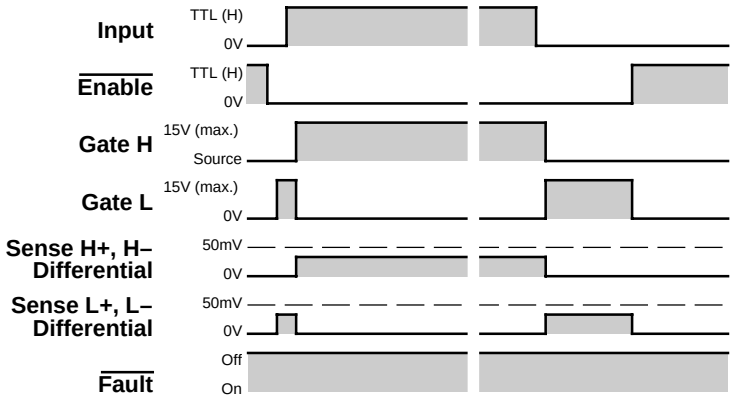


Input Current vs. Input Voltage

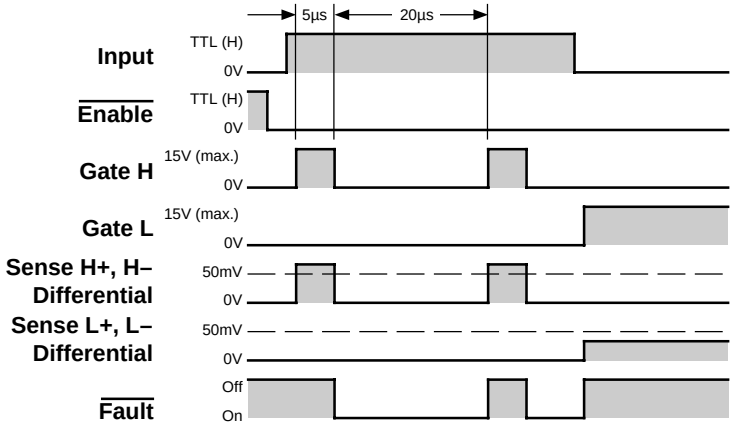


Sense Threshold vs. Temperature

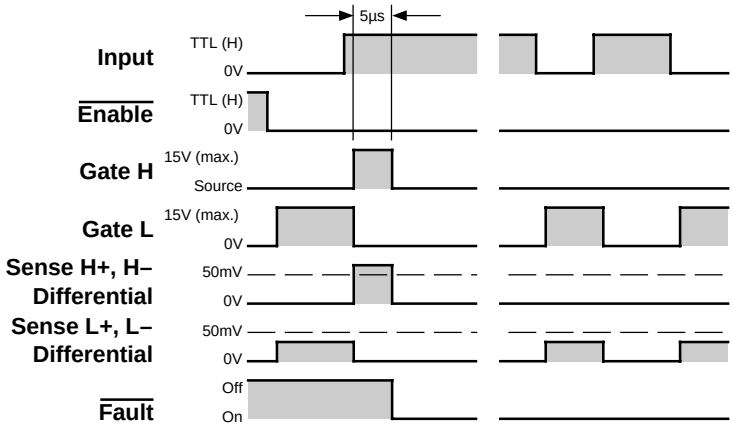




Timing Diagram 1. Normal Operation



Timing Diagram 2. Overcurrent Fault with Retry



Timing Diagram 3. Overcurrent Fault with Maintained Off

Functional Description

Refer to the MIC5022 block diagram.

Input

A signal greater than 1.4V (nominal) applied to the MIC5022 INPUT causes gate enhancement on an external MOSFET connected to GATE H turning the high-side MOSFET on.

At the same time internal logic removes gate enhancement from an external MOSFET connected to GATE L, turning the low-side MOSFET off.

An internal pull-down resistor insures that an open INPUT remains low, keeping the external high-side MOSFET turned off and the low-side MOSFET turned on.

Enable (Active Low)

A signal greater than 1.4V (nominal) applied to the MIC5022 $\overline{\text{ENABLE}}$ keeps both GATE outputs off. An internal pull-down resistor insures that the MIC5022 is enabled if the pin is open.

Gate Outputs

Rapid rise and fall times on the GATE output are possible because each input state change triggers a one-shot which activates a high-value current sink ($10I_2$) for a short time. This draws a high current though a current mirror circuit causing the output transistors to quickly charge or discharge the external FET's gate.

A second current sink continuously draws the lower value of current used to maintain the gate voltage for the selected state.

Internal 15V Zener diodes protect the external high-side and low-side MOSFETs by limiting the gate to source voltage.

Charge Pump (High-Side)

An internal charge pump utilizes an external "boost" capacitor connected between V_{BOOST} and the source of the external FET (refer to Typical Application). The boost capacitor stores charge when the FET is off. As the FET begins to turn on the voltage on the source side of the capacitor increases (because it is on the high side of the load) raising the V_{BOOST} pin voltage. The boost capacitor charge is directed through the gate pin to quickly charge the FET's gate to 15V maximum above V_{DD}. The internal charge pump maintains the gate voltage by supplying a small current as needed.

Overcurrent Limiting (High or Low-Side)

Current source I_1 charges C_{INT} upon power up. An optional external capacitor connected to C_T is kept discharged through a FET Q1.

A fault condition (> 50mV from SENSE + to SENSE –) causes the overcurrent comparator to enable current sink $2I_1$ which overcomes current source I_1 to discharge C_{INT} in about 5µs time. When C_{INT} is discharged, the INPUT is disabled, the FAULT output is enabled, and C_{INT} and C_T are ready to be charged. Since the INPUT is disabled the GATE output turns off.

When the GATE output turns off the FET, the overcurrent signal is removed from the sense inputs which deactivates current sink $2I_1$. This allows C_{INT} and the optional capacitor connected to C_T to recharge. A Schmitt trigger delays the retry while the capacitor(s) recharge. Retry delay is increased by connecting a capacitor connected to C_T (optional).

The MIC5022's low-side driver may be used without current sensing by grounding both SENSE + and SENSE – pins. The high-side driver may be used without current sensing by connecting SENSE + and SENSE – to the source of the external high-side MOSFET.

Fault Output

The FAULT output is an open collector transistor. FAULT is active at approximately the same time the output is disabled by a fault condition (5µs after an overcurrent condition is sensed). The FAULT output is open circuit (off) during each successive retry (5µs).

Typical Full-Bridge Application

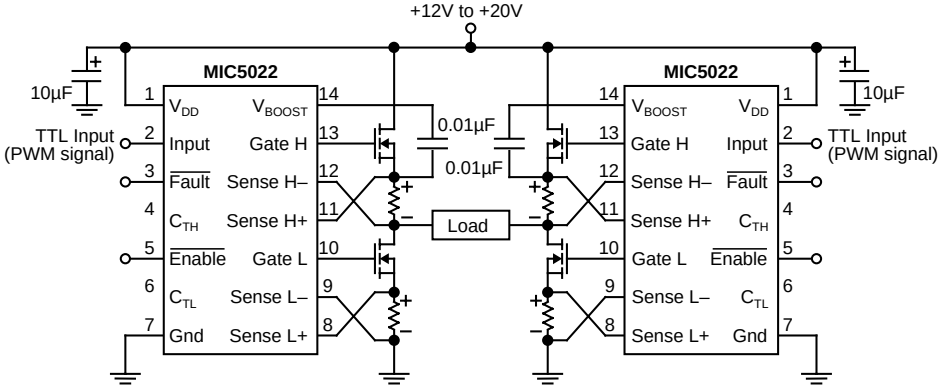


Figure 1. Basic Full-Bridge Circuit

Applications Information

The MIC5022 MOSFET driver is designed for half-bridge switching applications where overcurrent limiting and high speed are required. The MIC5022 can control MOSFETs that switch voltages up to 36V.

The MIC5022 functionally includes the MIC5020 and MIC5021 with additional circuitry to coordinate the operation of the high and low-side drivers. Since most output considerations are similar, *refer to the MIC5020 and MIC5021 data sheets for additional applications information.*

Supply Voltage

The MIC5022's supply input (V_{DD}) is rated up to 36V. The supply voltage must be equal to or greater than the voltage applied to the drain of the external N-channel MOSFET.

A 16V minimum supply is recommended to produce continuous on-state, gate drive voltage for standard MOSFETs (10V nominal gate enhancement).

When the driver is powered from a 12V to 16V supply, a logic-level MOSFET is recommended (5V nominal gate enhancement).

PWM operation may produce satisfactory gate enhancement at lower supply voltages. This occurs when fast switching repetition makes the boost capacitor a more significant voltage supply than the internal charge pump.

Overcurrent Limiting

Separate high and low-side 50mV comparators are provided for current sensing. The low level trip point minimizes I^2R losses when a power resistor is used for current sensing.

The adjustable retry feature can be used to handle loads with high initial currents, such as lamps or heating elements, and can be adjusted from the C_T connection.

C_T to ground causes maintained gate drive shutdown following an overcurrent condition.

C_T open, or a capacitor to ground, causes automatic retry. The default duty cycle (C_T open) is approximately 20% (the high side is slightly greater than the low side). Refer to the typical characteristics when selecting a capacitor for a reduced duty cycle.

C_T through a pull-up resistor to V_{DD} increases the duty cycle. *Increasing the duty cycle increases the power dissipation in the load and MOSFET under a "fault" condition.* Circuits may become unstable at a duty cycle of about 75% or higher, depending on conditions. *Caution: The MIC5022 may be damaged if the voltage applied to C_T exceeds the absolute maximum voltage rating.*

Boost Capacitor Selection

For 12V to 20V operation, the boost capacitor should be 0.01µF; and for 12V to 36V operation, the boost capacitor should be 2.7nF; both connected between V_{BOOST} and the MOSFET source. The preferred configuration for 20V to 36V operation is a 0.1µF capacitor connected between V_{BOOST} and V_{DD} . Refer to the MIC5021 data sheet for examples.

Do not connect capacitors between V_{BOOST} and the MOSFET source and between V_{BOOST} and V_{DD} at the same time. Larger capacitors than specified may damage the MIC5022.

Circuits Without Current Sensing

Current sensing may be omitted by connecting the high-side SENSE + and SENSE – pins to the source of the MOSFET or the supply and the low-side SENSE + and SENSE – pins to ground. Do not connect the high-side sense pins to ground.

Inductive Load Precautions

Circuits controlling inductive loads require precautions when controlled by the MIC5022. Wire wound resistors, which are sometimes used to simulate other loads, can also show significant inductive properties.

Sense Pin Considerations

The sense pins of the MIC5022 are sensitive to negative voltages. If a voltage spike is too negative (below approximately –0.5V), current will be drawn from functional sections of the IC resulting in unpredictable circuit behavior or damage. Resistors and Schottky diodes may be used to protect the sense pins from the negative spikes. Refer to the MIC5021 data sheet for details.

High-Side Sensing

For the high-side driver, sensing the current on the supply side of the high-side MOSFET locates the SENSE pins away from the inductive spike. Refer to the MIC5021 data sheet for details.

Low-Temperature Operation

As the temperature of the MIC5022AJB (extended temperature range version—no longer available) approaches –55°C, the driver's off-state, gate-output offset from ground increases. If the operating environment of the MIC5022AJB includes low temperatures (–40°C to –55°C), add an external 2.2MΩ resistor from gate-to-source or from gate-to-ground. This assures that the driver's gate-to-source voltage is far below the external MOSFET's gate threshold voltage, forcing the MOSFET fully off. Refer to the MIC5020 and MIC5021 data sheets for examples.

The gate-to-source configuration is appropriate for resistive and inductive loads. This also causes the smallest decrease in gate output voltage.

The gate-to-ground configuration is appropriate for resistive, inductive, or capacitive loads. This configuration will decrease the gate output voltage slightly more than the gate-to-source configuration.

Full-Bridge Motor Control

An application for two MIC5022s is the full-bridge motor control circuit.

Two high or two low-side sense inputs may be used for overcurrent detection. (Low-side sensing is shown in Figure 2). Sensing at four locations is usually unnecessary.

When switching inductive loads, such as motors, it is desirable to place the high-side sense inputs on the supply side of the MOSFETs. The helps prevent the inductive spikes that occur upon load shutoff from affecting the sense inputs.

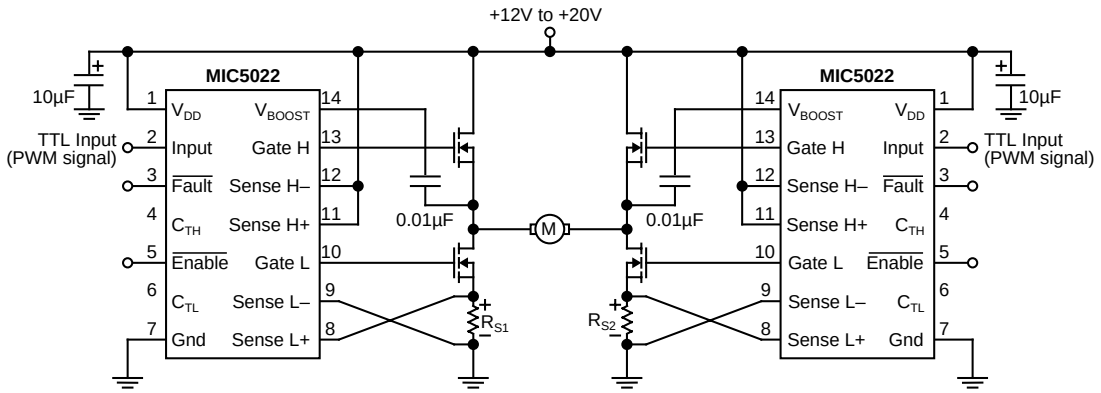


Figure 2. Full-Bridge Motor Control Application

Synchronous Rectifier Converter

The MIC5022 can be part of a synchronous rectifier in SMPS (switch mode power supply) applications.

This circuit uses the MIC38C43 SMPS controller IC to switch a pass transistor (Q1) and a "synchronous rectifier" transistor (Q2) using the MIC5022.

The MIC38C43 controller switches the transistors at 50kHz. Output regulation is maintained using PWM. When the pass transistor is on, the synchronous rectifier is off and current is forced through the inductor to the output capacitor and load. When the pass transistor is switched off, the synchronous rectifier is switched on allowing current to continue to flow as the inductor returns stored energy.

The synchronous rectifier MOSFET has a lower voltage drop than the forward voltage drop across a Schottky diode. This increases converter efficiency which extends battery life in portable equipment.

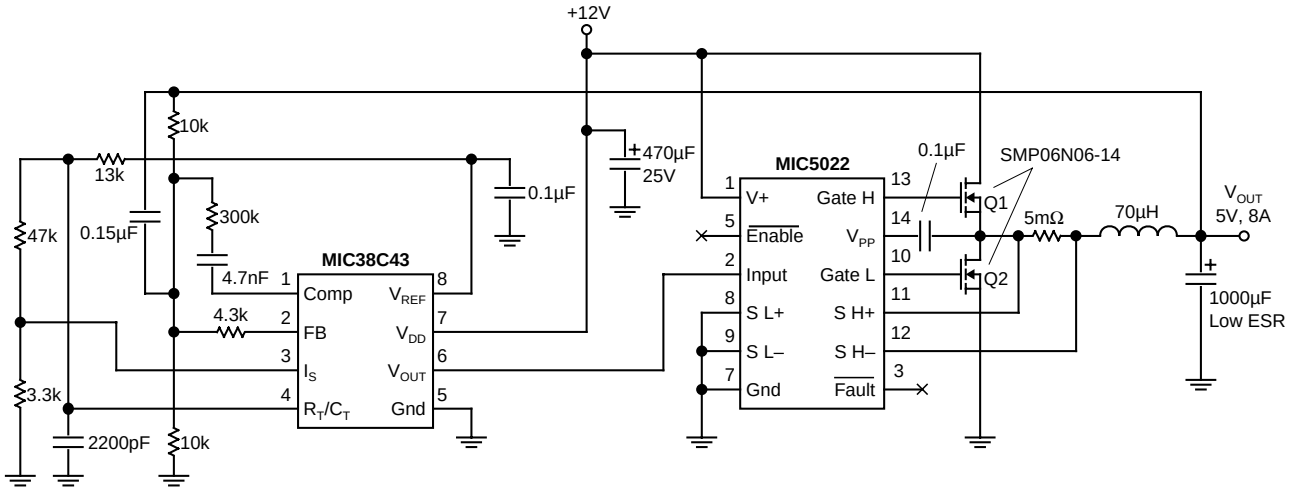


Figure 3. 50kHz Synchronous Rectifier Converter